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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Bednar et al.

Serial No.: 10/604,277 Filing Date: 7/8/2003

Art Unit: 2811

Dkt. No.: BUR920020092US1

Title: NESTED VOLTAGE ISLAND ARCHITECTURE

Assistant Commissioner for Patents Office of Initial Patent Examination Customer Service Center Washington, D.C. 20231

CORRECTION OF FILING RECEIPT

Sir:

7)

Applicants respectfully request correction of the filing receipt for this case as indicated on the attached copy of the filing receipt.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully submitted,

Date: October 31, 2003

Jack P. Friedman, Ph.D.

Reg. No. 44,688

I HEREBY CERTIFY THAT THE CORRESPONDENCE TO WHICH THIS STATEMENT IS AFFIXED IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE, POSTAGE PAID, AS FIRST CLASS MAIL, IN AN ENVELOPE ADDRESSED TO ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231 ON October 31, 2003

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
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CONFIRMATION NO. 1276

Date Mailed: 09/22/2003

FILING RECEIPT

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30449 SCHMEISER, OLSEN + WATTS SUITE 201 3 LEAR JET LATHAM, NY 12033

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appropriate).

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Assignment For Published Patent Application

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Early Publication Request: No

COCKETE



Title

NESTED VOLTAGE ISLAND ARCHITECTURE

Preliminary Class

257

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